

# Accelerating The Creation of Semiconductors

## Corporate Overview

Charlie Janac  
CEO

Nick Hawkins  
CFO

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**ARTERIS** 

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# Macro Factors Driving Arteris Growth

**ARTERIS** IP Growth Opportunities

## MACRO Trends

Artificial Intelligence. Machine Learning. Gen AI. LLMs.



Electrification. Energy Efficiency. Green Tech. Sustainability.

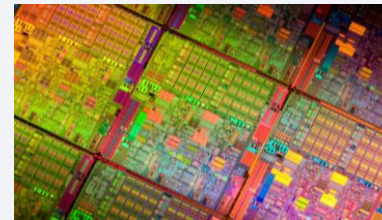


Regionalized & Government Investments.

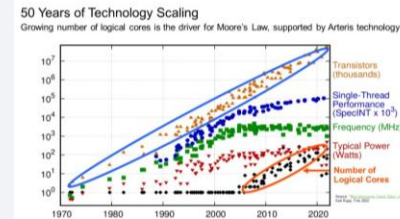


## INDUSTRY Trends

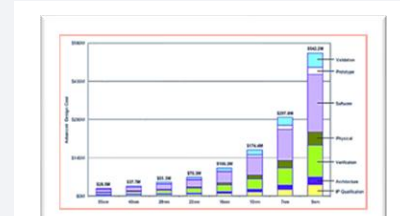
Advanced Nodes, \$1T Semi by 2030



Growing Chip Size/Complexity. Growing IP & NoC Content.

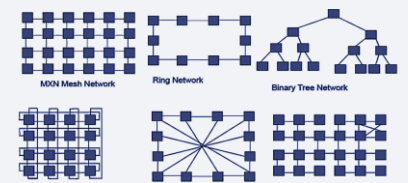


SoC Development Costs. Talent Scarcity

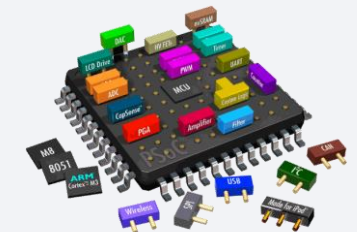


## DESIGN Trends

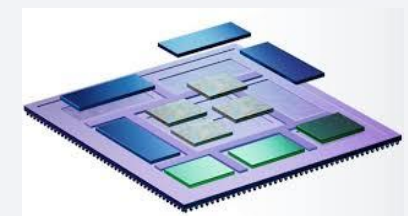
NoC Complexity.



SoC Connectivity.



Multi-Die. Chiplets.



# SoCs are made from IP Blocks → Commercial and Internal

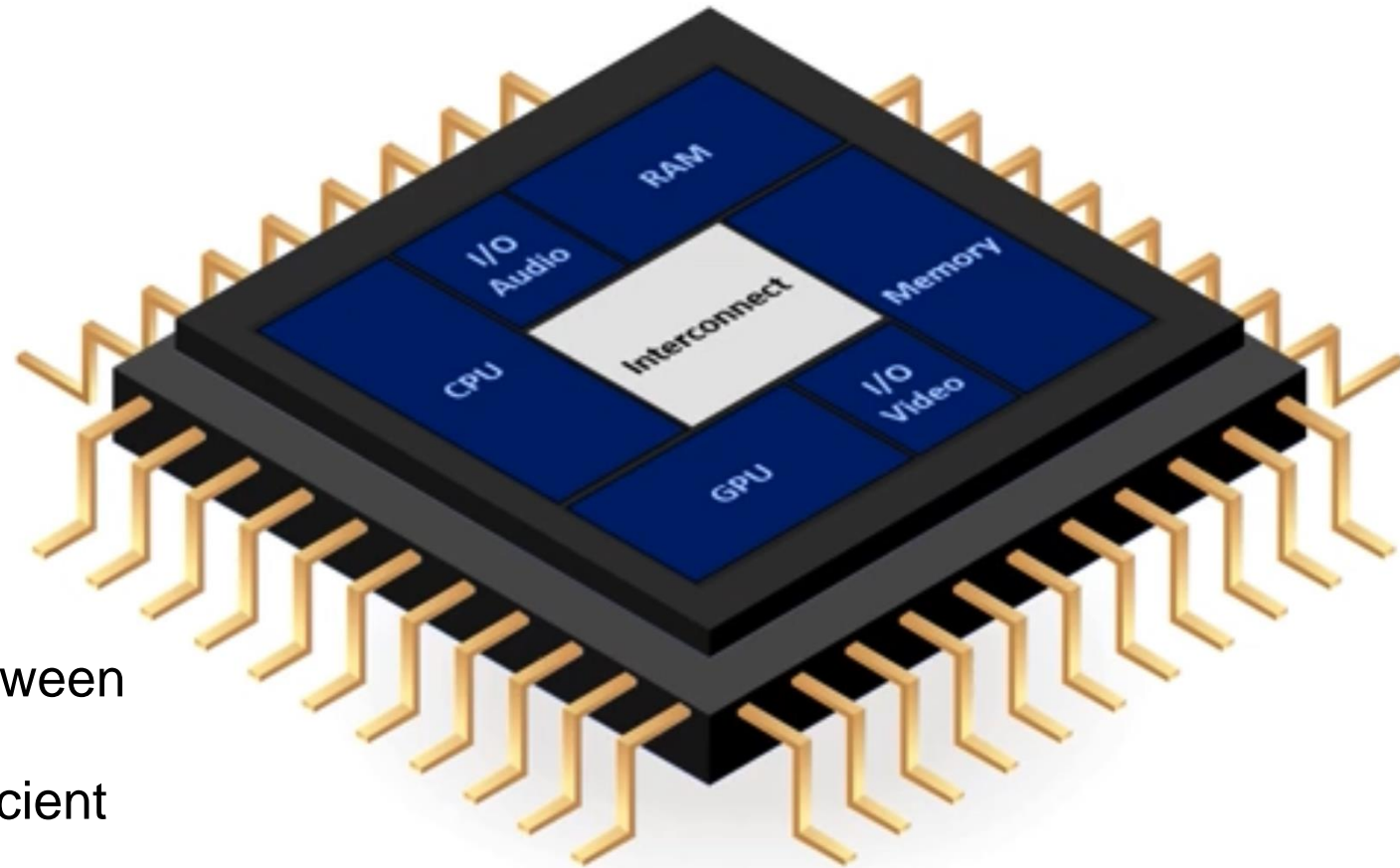
Printed circuit boards became chips, chips become chiplets → SoC/SIPs become electronic systems

## ■ Arteris Network-on-Chip IP connecting:

- Non-Coherent NoC → FlexNoC<sup>®</sup>
- Cache Coherent NoC → Ncore<sup>®</sup>
- Last Level Cache → Codacache<sup>®</sup>

## Subsystem NoCs

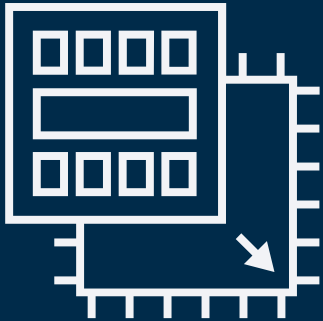
- Memory Subsystem
  - NPU Subsystem
  - Video Subsystem
  - PCIe Subsystem
  - Safety Island Subsystem
- 
- Establishing high-level connectivity between client IP blocks → Magillem
  - Configuring IP port register RTL for efficient Hardware Software Int. → Semifore



# Arteris' Market Definition → Developing the System IP Market

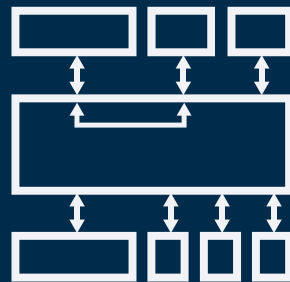
## NoC Interconnect IP

Protocol converters, switches, rate adaptors, etc.  
Carries most of SoC data



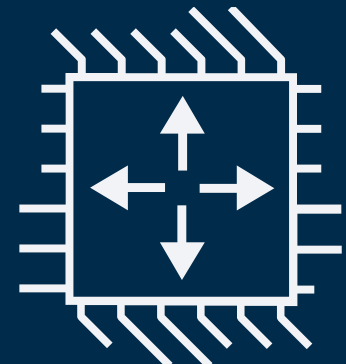
## NoC Interface IP

SoC IP blocks connected to NoC IPs to improve SoC performance & functionality



## SoC Integration Automation

Software to package & configure client IP blocks to integrate with NoC IPs



# Arteris – A Leading SoC System IP Company

Global customer base deploying Arteris interconnect IP and SoC Integration Software

- Silicon-proven IP used in ~3.5 billion+ SoCs shipped to date
- 200+ customers and 725+ SoC design starts to date
- 70-80% market share of automotive ADAS SoC market<sup>1</sup>
- Strong presence in Artificial Intelligence/Machine Learning (AI/ML) system IP
- Broad interoperability - any processor, any IP, any EDA, any foundry
- Innovative technology coupled with expert support results in a 90+% customer retention rate
- 71 patents and 77 patent applications
- ISO 9001:2015 Quality Management System (QMS) Certified

<sup>1</sup> Management estimates

## Diversified Customer Base

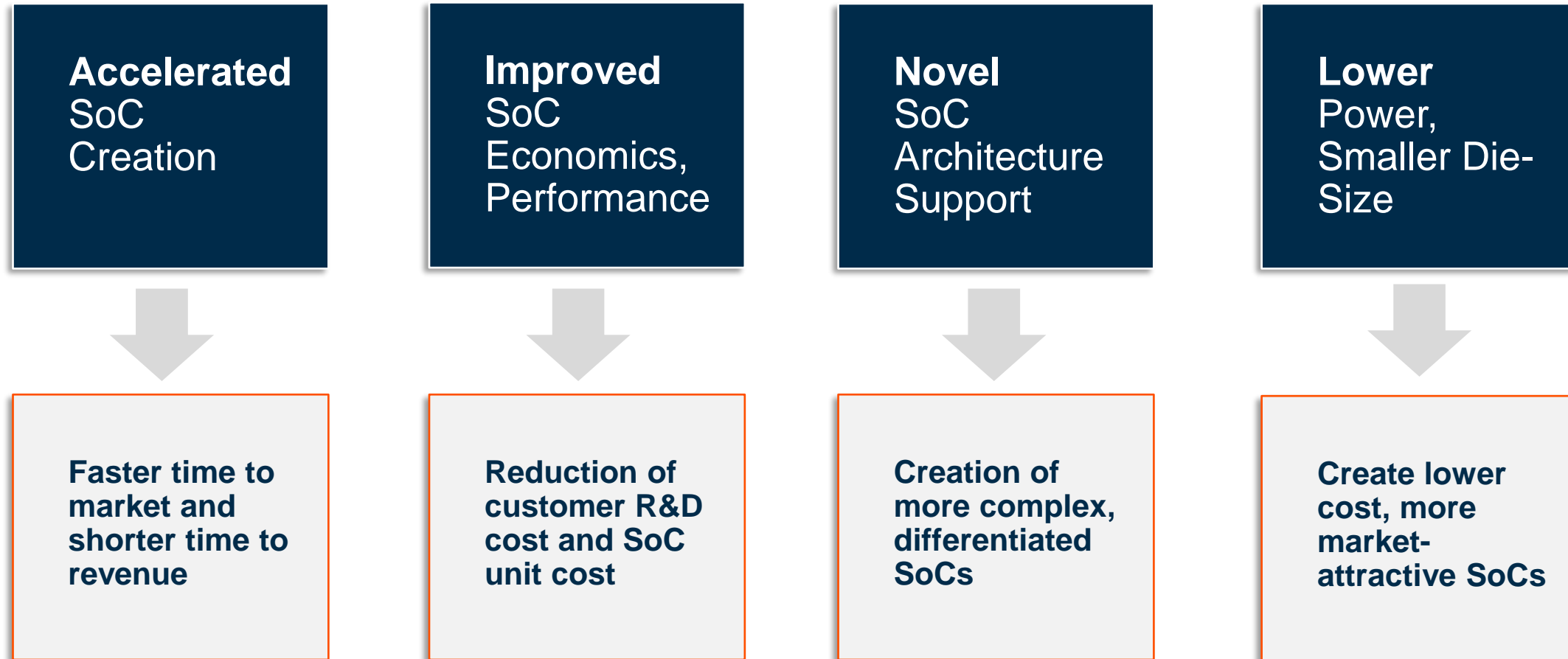
*Subset of Publicly Disclosed Customers*





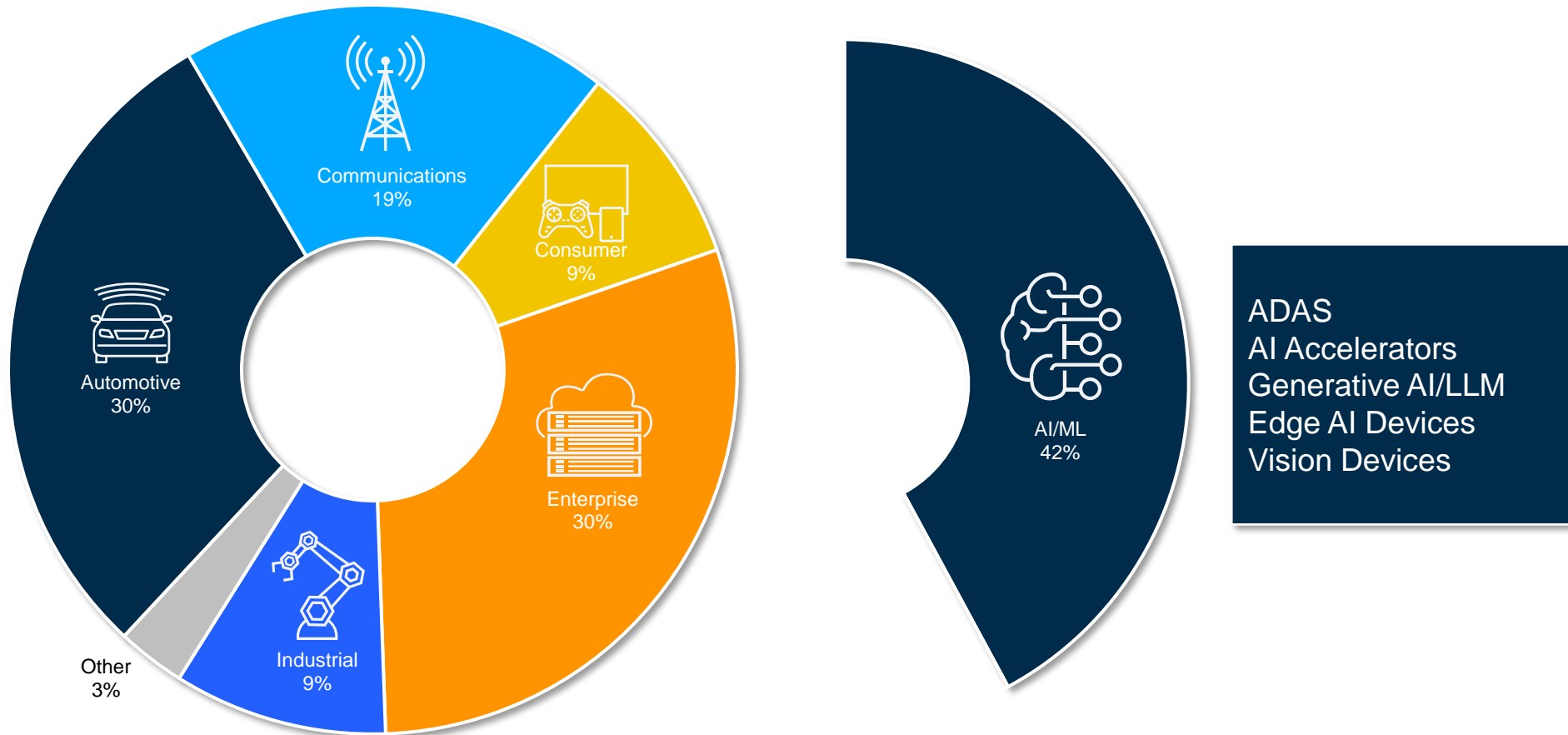
# Technology & Economic Factors Driving Arteris' Customer Adoption

Enabling customers to create complex SoCs efficiently and reliably



# Accelerating Innovation in Key Verticals & Horizontals

All SoCs need System IP Solutions – A chip must communicate to be a chip





# Artificial Intelligence/Machine Learning (AI/ML) Horizontal

**AI Chip Market:  
~3x Increase from 2022 to 2027<sup>1</sup>**



**2022 AI-enabled  
applications  
processors: \$44B<sup>1</sup>**

**2027 AI-enabled  
applications  
processors:  
\$119B<sup>1</sup>**

**Generative AI  
56% CAGR<sup>2</sup>**

- Generative AI is a revolution in man/machine interface technology
- Increasing number of industry AI ASICs, meeting high data bandwidth and unique feature requirements
- Multiple Generative AI ASICs in design incorporating Arteris system IP

Arteris Customers → 180+ Design Wins

Data Center  
**Hyperscalers**  
(subject to NDAs)  
**Bitmain**  
**Neureality**

Edge  
**Renesas**  
**NXP**  
**Sima.ai**  
**Axelera**

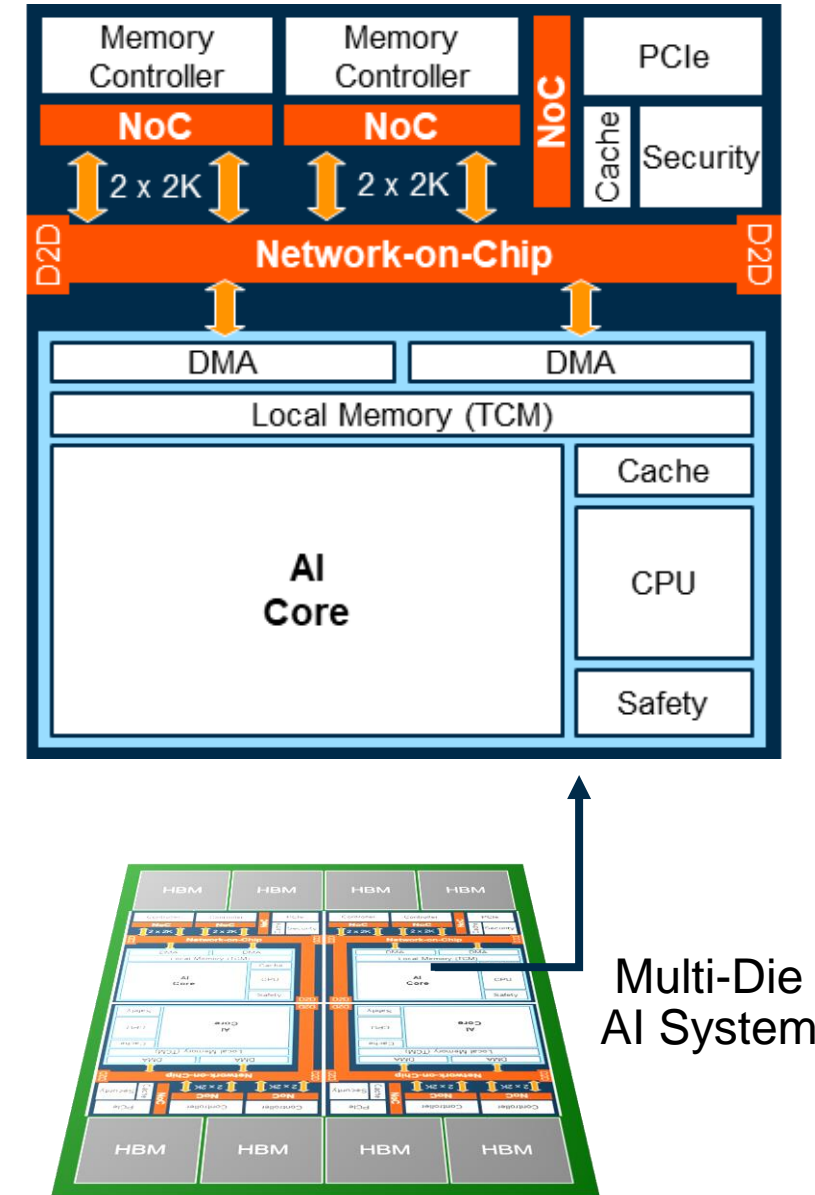
Endpoint  
**Mobileye**  
**Socionext**  
**Hailo**

1. Source: Gartner  
2. CAGR 2023 – 2028; Source: Omdia Informa

# Generative AI Data Transport Architecture

Arteris FlexNoC with XL Option for Gen AI, LLM applications

- A tremendous amount of data moved in Gen AI chips
- Maximizing Throughput to Handle Trillion + Parameter AI
- Reduce data movement by bringing compute and memory
- Performance Scaling for Multi TFlops/GHz
- Support of Arm, RISC-V, and mixed architectures
- Support of Multi-Die / chiplet architectures
- Efficient movement of data improves power and performance



Multi-Die AI System

# NeuReality Inference Server, with NR1 SoC connected by Arteris Targeting Generative AI and Large Language Model (LLM) Applications

## Drivers

- Increasing demand for hardware solutions optimized to handle very large data requirements of Generative AI with Large Language Model applications

## AI/ML Collaboration

- NeuReality's Network Addressable Processing Unit (NAPU), a network-attached heterogeneous chip for complete AI-pipeline offloading
- Arm Neoverse N1 processor IP cores to host Linux-based server applications with native Kubernetes for cloud and data center orchestration
- Arteris 8-hierarchy NoC with an aggregated bandwidth of 4.5TB/sec

## First Deliverable

- NeuReality NR1 SoC connected by Arteris FlexNoC interconnect IP
- NeuReality NR1-S™ AI Inference Server with NR1 SoCs



Read more here: [NeuReality NR1 Inference Server](#), [Arteris AI/ML Collaboration](#)

# Automotive Vertical

**AUTOMOTIVE SoC**  
**19% CAGR<sup>1</sup>**



**ADAS**  
**31% CAGR<sup>1</sup>**

**Connectivity/ Telematics**  
**11% CAGR<sup>2</sup>**

**Auto HPC**  
**(High Performance Compute)**  
**99% CAGR<sup>1</sup>**

**Infotainment**  
**8% CAGR<sup>2</sup>**

1. CAGR 2022 – 2030; Source: Gartner  
2. CAGR 2022 – 2026; Source: Omdia Informa






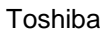


















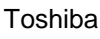








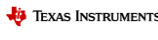














- 130+ SoC design wins, OEMs take on silicon
- ~\$117 billion automotive semiconductor market by 2030<sup>1</sup>
- Partnered with **Arm** in Automotive
- Selected by 5 major **Auto OEMs** in 2023
- Unique **Safety** capabilities

## Arteris Customers

BMW  
NXP  
Mobileye  
Dreamchip  
Many others subject to NDA

# Arteris' Position in Automotive Transformation → Internet of Cars

## Arteris' System IP enables novel automotive SoC architectures

SoCs per Function		Arteris IP Customers → 130+ SoC design wins						
ADAS / Machine Learning / Car Controller (1-4 systems per vehicle)	2	 Horizon Robotics  RECOGNITION HEALTHCARE RECOGNITION  BOSCH	 mobileye™  socionext™  Toshiba	 Major Automotive EV OEM  NXP®  AutoChips	 HAILO  BLACK SESAME TECHNOLOGIES  Major Design Services Company  SEM(DR)VE 芯燻科技	 Telechips  indie  Major ADAS System Maker	 ST life.augmented  bos SEMICONDUCTORS  Dream CHIP	
Vision Camera – Local Processing (4-16 systems per vehicle)	4	 mobileye™	 BLACK SESAME TECHNOLOGIES	 tenstorrent	 nextchip	 TEXAS INSTRUMENTS	 Toshiba	
Radar / Lidar	6	 arbe	 CALTEK	 NXP®	 vayyar™	 AEVA	 BOSCH	 UHNDER
Infotainment	1	 NXP®	 TEXAS INSTRUMENTS	 Major FPGA Company #1	 bos SEMICONDUCTORS	 Major FPGA Company #2	 Telechips	
Dashboard / HUD / DMS	2		 NXP®	 sienqine 芯燻科技 Technology	 RENESAS			
Chassis / Engine / Motor Control	5			 ST life.augmented	 indie			
V2X / V2I / WAN Modem / Gateway	3		 NXP®	 Autotalks	 MORNINGCORE 晨芯科技	 SEQUANS	 Silicon Mobility	

Source: IHS Markit, McKinsey

**23** average complex SoCs per electronically-enabled vehicle by 2026

# 12 Year Relationship Between Mobileye and Arteris

Meeting stringent requirement of automotive ADAS SoCs

## Growth of Mobileye ADAS SoC Complexity 2010- 2021

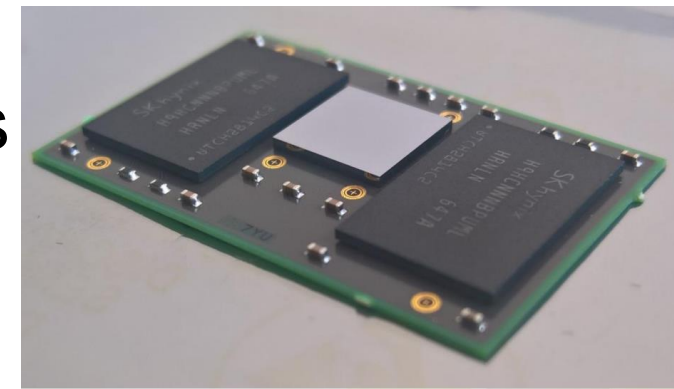


•Arteris IP Inteconnect in Mobileye for 10 years

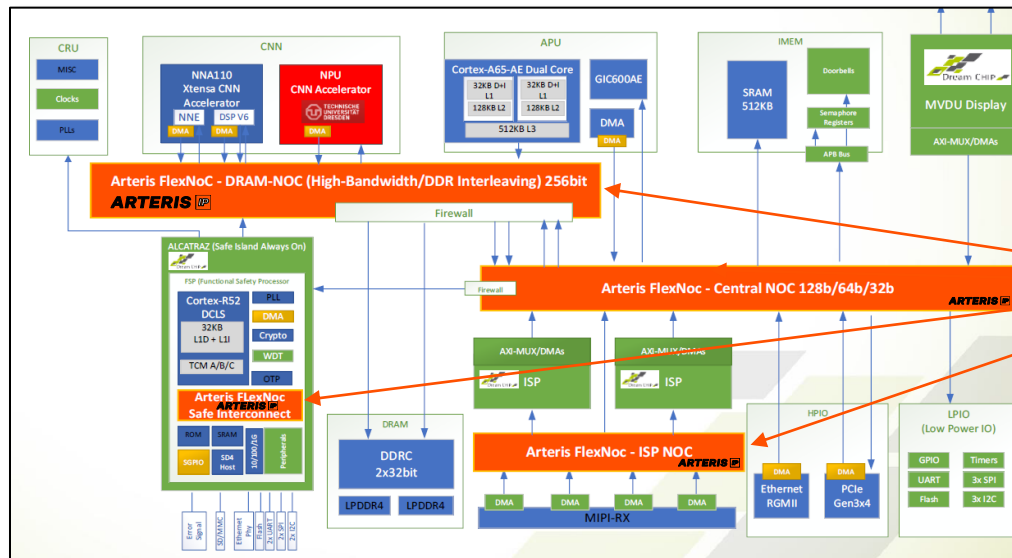
- Reasons for Adoption
  - Superior NoC Performance
  - Superior NoC
  - Flexibility
  - Low NoC power consumption
  - Unique cache coherency features
  - Attentive support
  - Automotive feature focus
  - Proven record of delivery
  - Architectural Flexibility



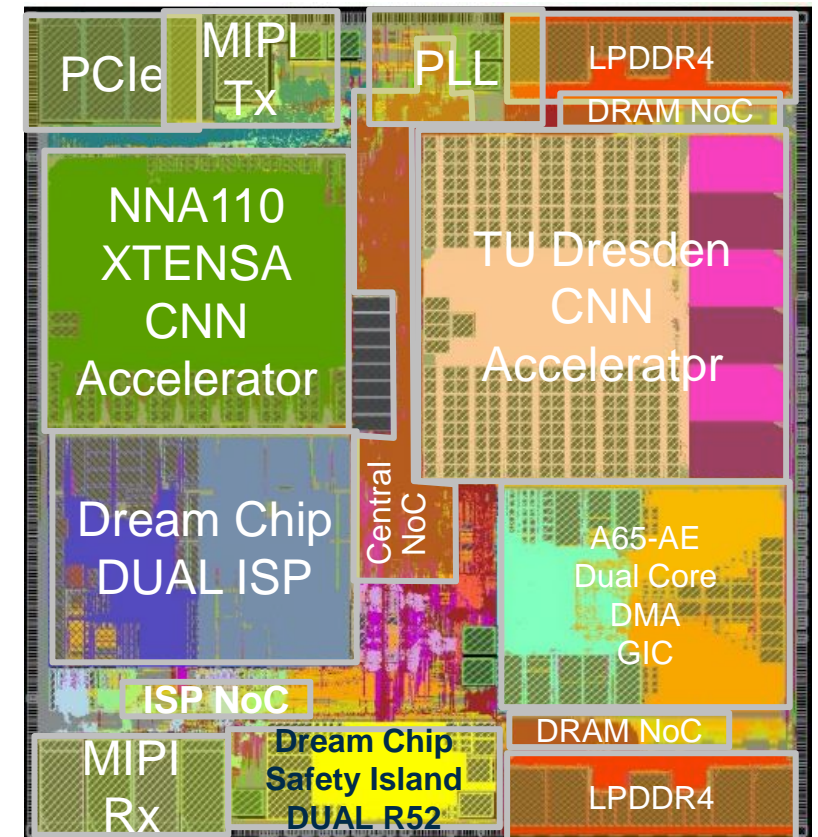
# DreamChip Automotive AI SoC, Connected by Arteris Production Level 2+ ADAS SoC with 2 machine learning sections



- Multiple Arteris Network-on-Chip IP instances
- 2 AI accelerators with 10 TOPS aggregated performance
- 2 DreamChip Image Signal Processors (ISPs)
- Arm Cortex-R52 based functional safety processor
- Dual-core Arm Cortex-A65AE processor cluster
- TÜV Süd certified for ISO26262 Safety, up to ASIL-D



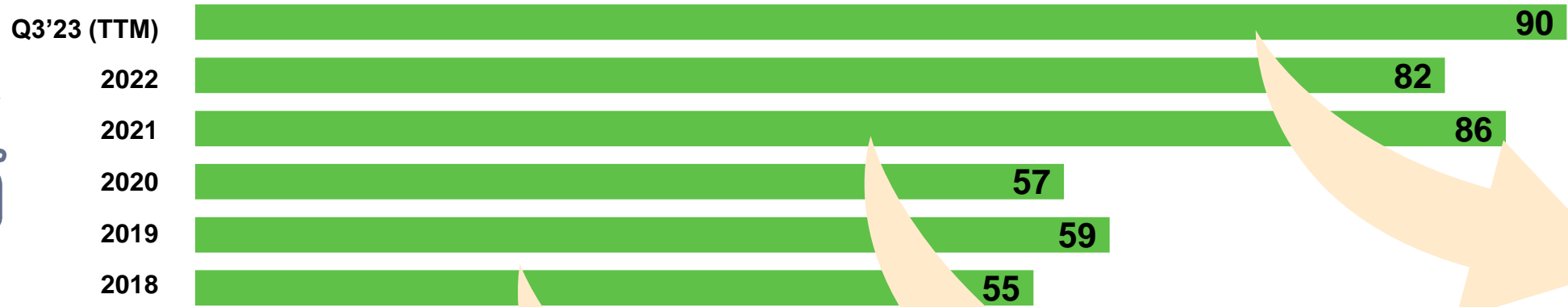
Multiple Arteris NoC IP Instances





# Growth in Confirmed Design Starts Drives Future Royalty Expansion

## Confirmed Design Starts<sup>3</sup>



Auto

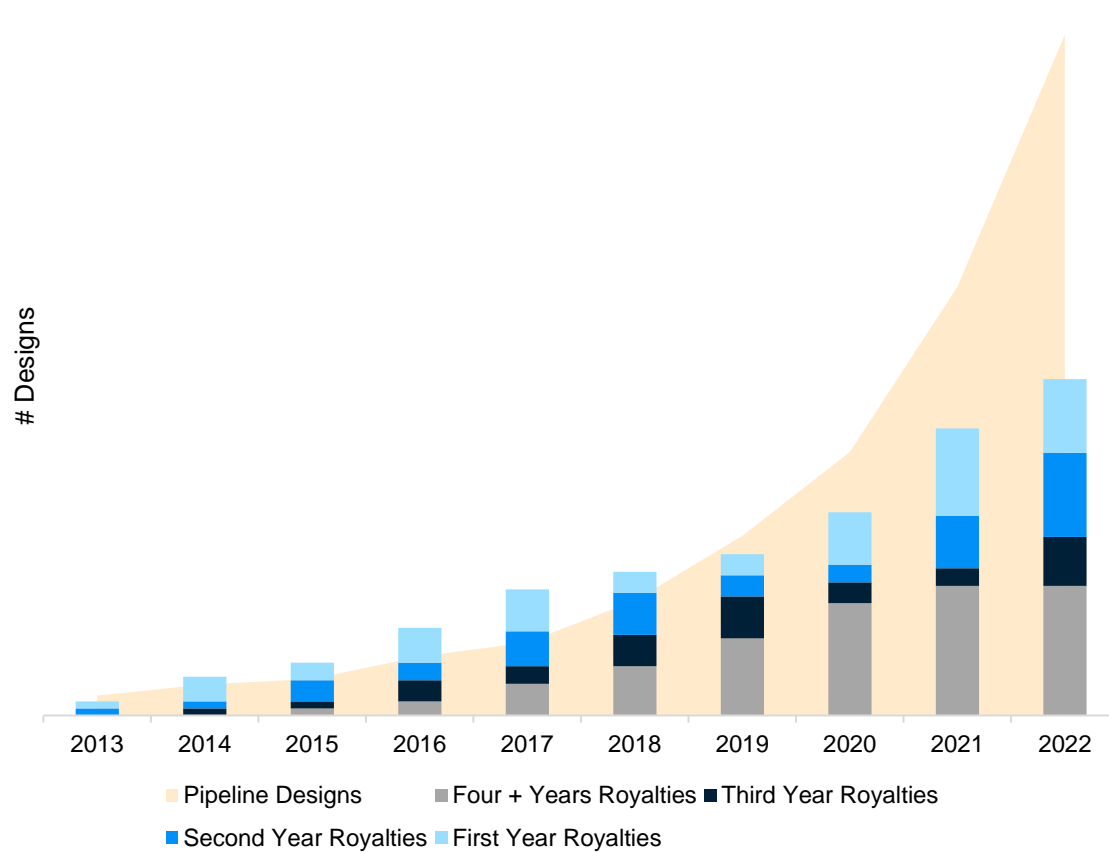
Royalty  
\$

Other

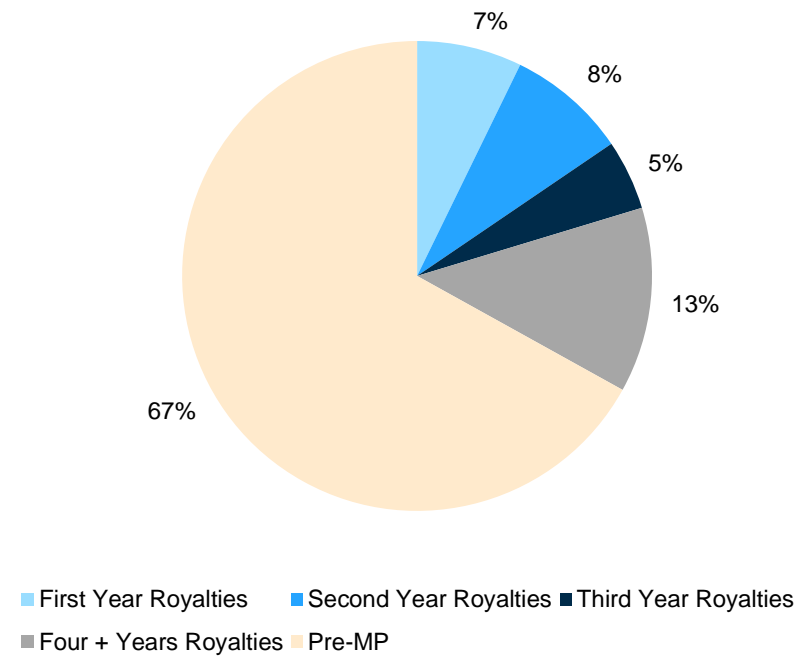
<sup>3</sup> We define Confirmed Design Starts as when customers confirm their commencement of new semiconductor designs using our interconnect IP and notify us

# A Growing Royalty Base

## Royalty Pipeline



## Royalty Design Maturity



# Growth Strategies and Milestones

**Organic product portfolio expansion**

- **June 2023** – FlexNoC 5 production shipments

**Focus on high growth market segments**

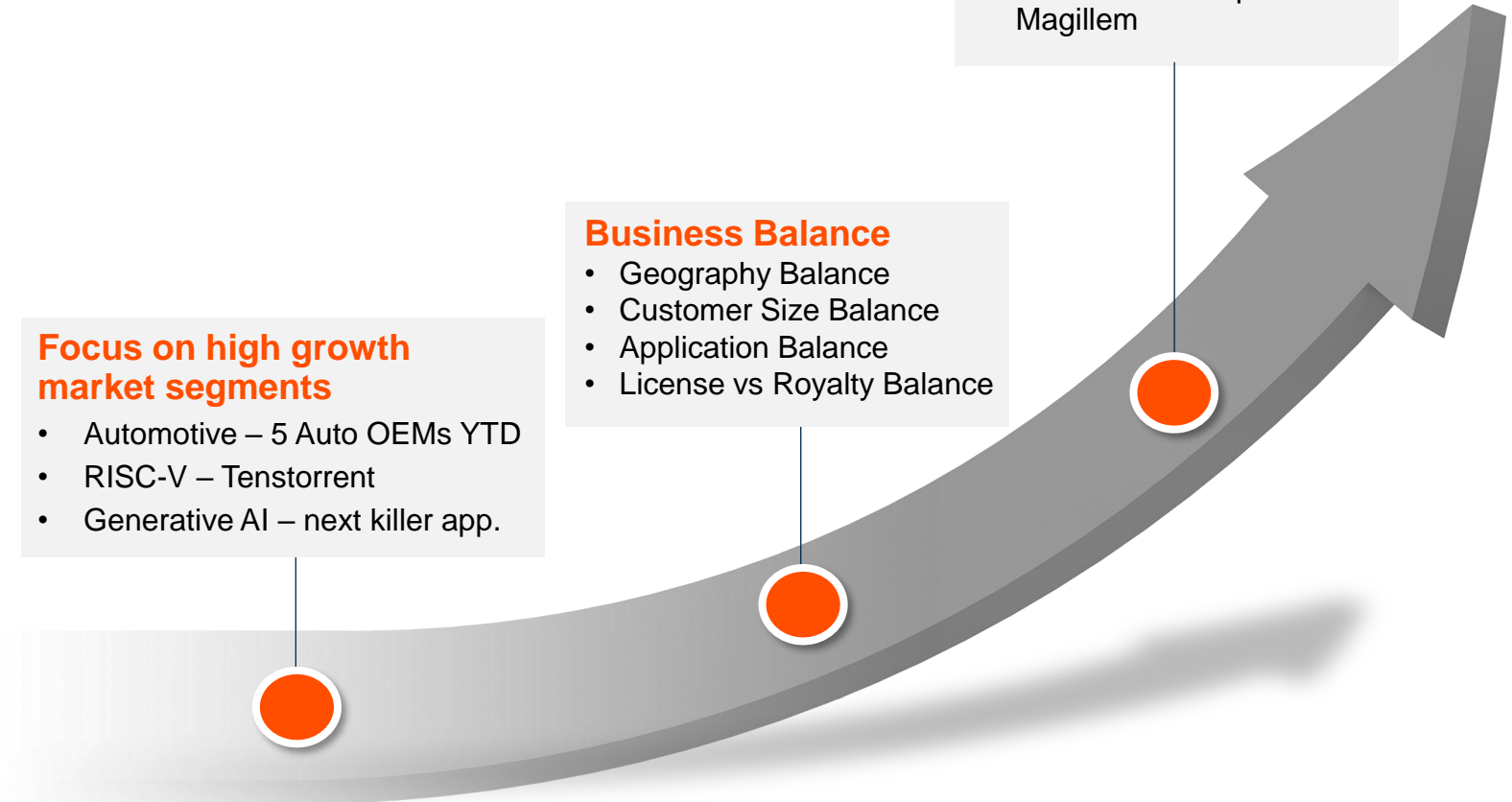
- Automotive – 5 Auto OEMs YTD
- RISC-V – Tenstorrent
- Generative AI – next killer app.

**Business Balance**

- Geography Balance
- Customer Size Balance
- Application Balance
- License vs Royalty Balance

**Inorganic growth**

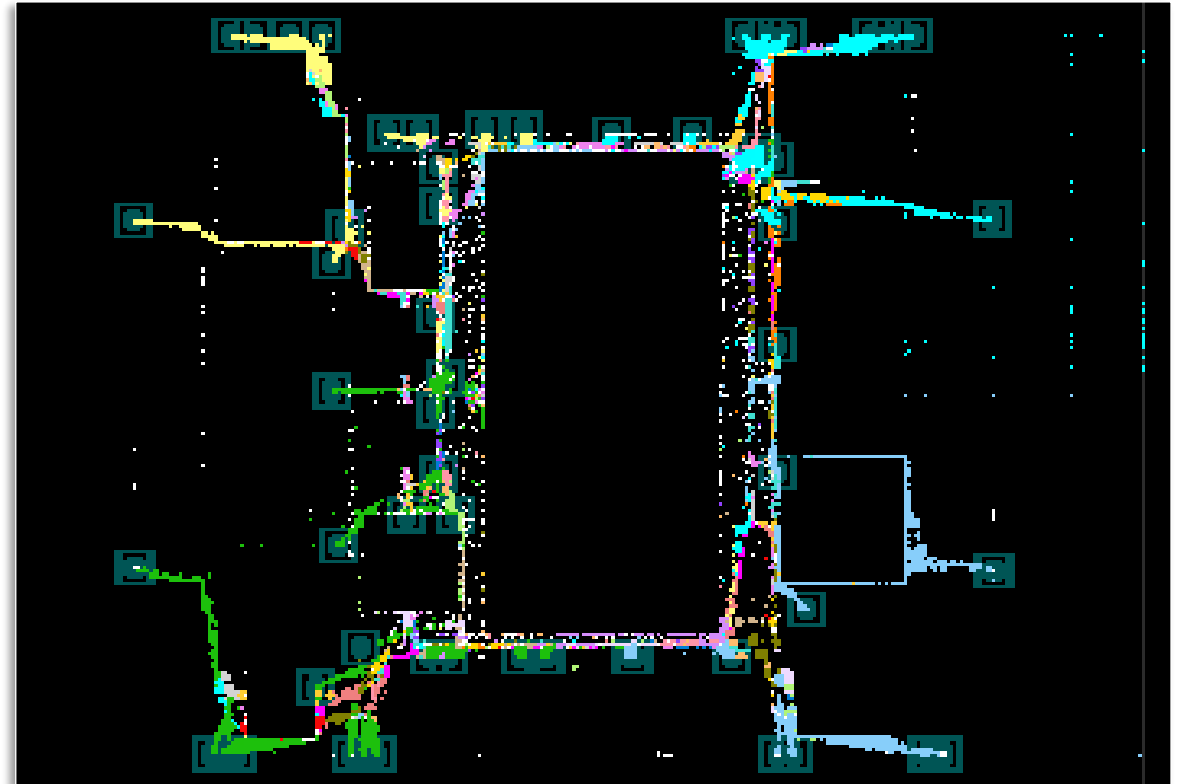
- **Dec. 2022** – Acquisition of Semifore
- **Dec. 2020** – Acquisition of Magillem



# Latest Product Innovation: FlexNoC 5 Network-on-Chip IP

One of the Industry's First ***Physically Aware*** NoC IP Designed To Reduce Complexity + Optimize Design

1. Customers get to **physical convergence up to 5X faster**.
2. Engineering resources are optimized, **reducing manual iterations**, cutting months to days.
3. Power, performance, and area (PPA) goals are achieved **within schedule and budget constraints**.
4. Solid customer adoption YTD
  - 9 FN5 customers through 3Q23 (first quarter of availability)
  - Numerous FN5 evaluations



## Financial Highlights

**Strong royalty model** Fueled by automotive & other verticals growth

**\$63M** Contracted future revenue (RPO)

**17%** CAGR in ACV  
9/30/20 – 9/30/23

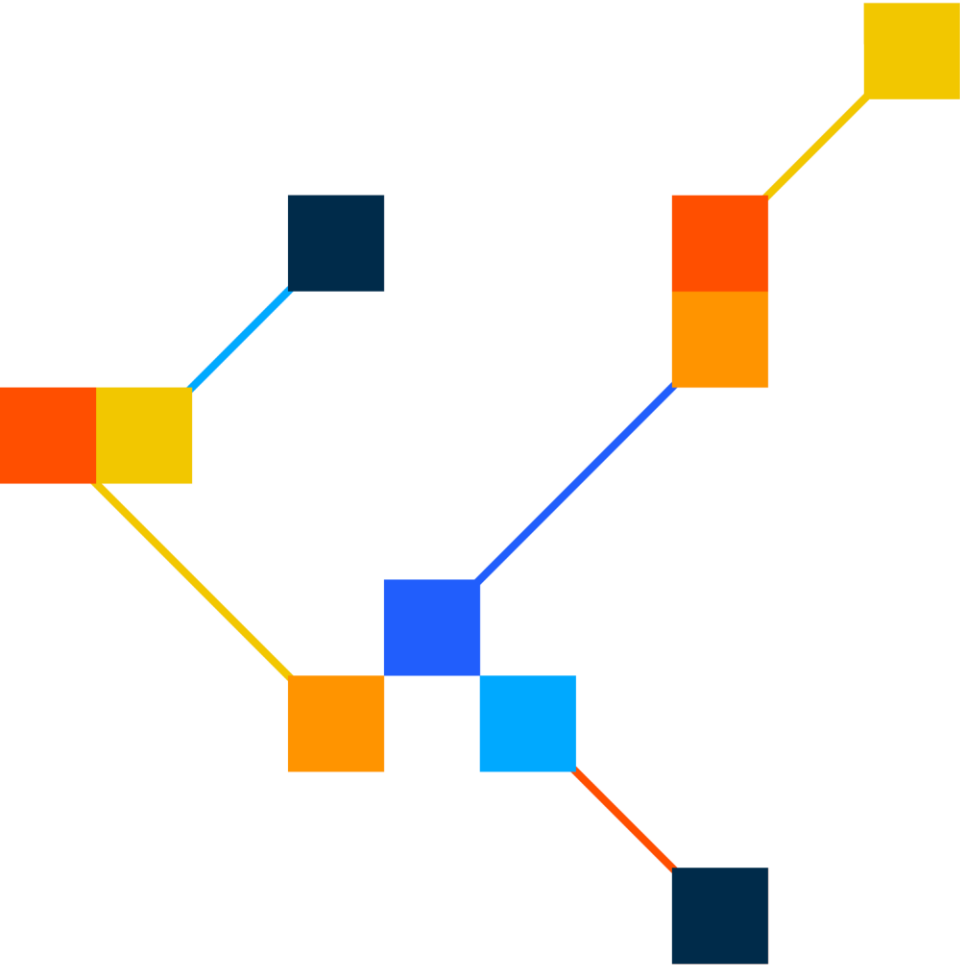
**90–95%** Gross Margin<sup>1</sup>

**Low Concentration** Region, customer, product origin

**Significant operating leverage**

**Debt free with Strong Cash Balance**

<sup>1</sup>2020-2022



**ARTERIS** **IP**

Thank you

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