Arteris Network-on-Chip Tiling Innovation Accelerates Semiconductor Designs for AI Applications

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Highlights:

- ***Scalable Performance:*** *Expanded network-on-chip tiling supported by mesh topology capabilities in FlexNoC and Ncore interconnect IP products allow systems-on-chip with AI to easily scale by more than 10 times without changing the basic design, meeting AI's huge demand for faster and more powerful computing.*
- ***Power Reduction:*** *Network-on-chip tiles can be turned off dynamically, cutting power by 20% on average, essential for more energy-efficient and sustainable AI applications with lower operating costs.*
- ***Design Reuse:*** *Pre-tested network-on-chip tiles can be reused, cutting the SoC integration time by up to 50% and shortening the time to market for AI innovations.*

CAMPBELL, Calif., Oct. 15, 2024 (GLOBE NEWSWIRE) -- Arteris, Inc. (Nasdaq: AIP), a leading provider of system IP which accelerates system-on-chip (SoC) creation, today announced an innovative evolution of its network-on-chip (NoC) IP products with tiling capabilities and extended mesh topology support for faster development of Artificial Intelligence (AI) and Machine Learning (ML) compute in system-on-chip (SoC) designs. The new functionality enables design teams to scale compute performance by more than 10 times while meeting project schedules plus power, performance and area (PPA) goals.

Network-on-chip tiling is an emerging trend in SoC design. The evolutionary approach uses proven, robust network-on-chip IP to facilitate scaling, condense design time, speed testing and reduce design risk. It allows SoC architects to create modular, scalable designs by replicating soft tiles across the chip. Each soft tile represents a self-contained functional unit, enabling faster integration, verification and optimization.

Tiling coupled with mesh topologies within Arteris' flagship NoC IP products, FlexNoC and Ncore, are transformative for the ever-growing inclusion of AI compute into most SoCs. AI-enabled systems are growing in size and complexity yet can be quickly scaled with the addition of soft tiles without disrupting the entire SoC design. Together, the combination of tiling and mesh topologies provides a way to further reduce the auxiliary processing unit (XPU) sub-system design time and overall SoC connectivity execution time by up to 50% versus manually integrated, non-tiled designs.

The first iteration of NoC tiling organizes Network Interface Units (NIUs) into modular, repeatable blocks, improving scalability, efficiency and reliability in SoC designs. These SoC designs result in increasingly larger and more advanced AI compute which supports fast-growing, sophisticated AI workloads for Vision, Machine Learning (ML) models, Deep Learning (DL), Natural Language Processing (NLP) including Large Language Models (LLMs), and Generative AI (GAI), both for training and inference, including at the edge.

"Thanks to Arteris' highly scalable and flexible mesh-based NoC IP, our SoC team has implemented support for larger AI data volumes and complex algorithms more efficiently. The close collaboration with Arteris has enabled us to create an Arm-based, multi-modal, software-centric edge AI platform that supports models ranging from CNNs to multimodal GenAI and everything in between with scalable performance per watt," said Srivi Dhruvanarayan, VP of hardware engineering at SiMa.ai. "We look forward to deploying the expanded Arteris NoC tiling and mesh functionality, which should further enhance our ability to create highly scalable AI silicon platforms for the edge."

"Arteris is continuously innovating, and this revolutionary NoC soft tiling functionality supported by large mesh topologies is an advancement in SoC design technology," said K. Charles Janac, president and CEO of Arteris. "Our customers, who are already building leading-edge AI-powered SoCs, are further empowered to accelerate the development of much larger and more complex AI systems with greater efficiency, all while staying within their project timeline and PPA targets."

The FlexNoC and Ncore NoC IP products, which offer expanded AI support via tiling and extended mesh topology capabilities, are now available to early-access customers and partners. To learn more, visit arteris.ai.

About Arteris

Arteris is a leading provider of system IP for the acceleration of system-on-chip (SoC) development across today's electronic systems. Arteris network-on-chip (NoC) interconnect IP and SoC integration automation technology enable higher product performance with lower power consumption and faster time to market, delivering better SoC economics so its customers can focus on dreaming up what comes next. Learn more at arteris.com.

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